Trends in Mobile Phones Processor Architecture

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ABSTRACT

Mobile phones, cell phone or hand phone, sometimes shortened to simply mobile, cell or just phone, has become one of the most necessity of our life. This study therefore, investigates the trends in the technology advancements which have resulted in significant changes in the processor architecture causing the transition from analog to digital telephony. The transformation in mobile phones devices has resulted in a wide range of data services. Processor architecture in mobile phones has become much more complex to satisfy performance such as communication speeds, display resolution, graphics, storage capacity, applications Processing and additional features such as Touch screens, Wi-Fi connectivity, motion control, enhanced I/O. The purpose of this paper is to review various processor architectures for mobile phones that has transformed the typical mobile phones of 90's to modern smart phones we have in use today.

Keywords: Cellular phones, Microprocessors, Graphics, Digital cameras, Multimedia systems, Multimedia databases, Processor architecture, DSP, VLIW, SoC, ARM processors

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1. BACKGROUND TO THE STUDY

Smartphones are a class of mobile phones and of multi-purpose mobile computing devices. They are distinguished from feature mobile phones by their stronger hardware capabilities and extensive mobile operating systems, which facilitate wider software, internet including web browsing over mobile broadband, and multimedia functionality such as music, video, cameras, and gaming, alongside core phone functions such as voice calls and text messaging. It typically includes various sensors that can be leveraged by their software, such as a magnetometer (instrument that measures magnetism e.g. compass), proximity sensors (a sensor able to detect the presence of nearby objects without any physical contact), barometer, gyroscope (device used for measuring or maintaining orientation and angular velocity) and accelerometer (device that measures proper acceleration) and support wireless communications protocols such as Bluetooth, Wi-Fi, and satellite navigation. In the past, mobile phones were mostly about making phone calls. They had a number pad, a digital phone book and a pick-up/hang-up button and not much more. Now smartphones offer so much more – they're really fully-fledged computers that you can fit in your pocket. They can run programs and games, access the internet, send email and much more.

Nearly all smartphones now use touchscreen controls. Instead of having hardware buttons like before, one side of the phone is taken up mostly by a touchscreen that you control using taps and gestures. There aren't even any number buttons; when you want to make a call, a number pad will pop up on the touchscreen. Becoming familiar with a smartphone can take a little bit of practice. But when you do become familiar with it, you'll find that a smartphone can do more than you ever thought possible on a mobile phone.

1.1 A Brief History of Smartphones

The first smartphones, the IBM Simon and Nokia Communicator 9000 were released way back in 1994 and 1996 respectively, and integrated the features of a mobile phone and a personal digital assistant (PDA) for managing calendars and contacts. Both were much larger than regular phones. It wasn't until 2000 that the first real smartphone, the Ericsson R380, was released. It wasn't any larger than a regular phone, and in the early 2000s many others followed suit, with phones like the Palm and BlackBerry achieving big success. In 2007, Apple released the iPhone, which eschewed hardware buttons for full touchscreen control and has been the template for smartphones ever since.

2. MOBILE PROCESSOR ARCHITECTURE TRENDS

The number of microprocessors sold in the world is now dominated by communication and embedded applications. Embedded microprocessors are now present in TV sets, DVD recorders, hi-fi sets, microwave ovens, washing machines, refrigerators, and in cars. A top of the line BMW features some 60 to 70 microprocessors which are used to control the brakes, the air bags, the windows, etc. It has been calculated that every American household owns around 60 microprocessors embedded in mobile devices and in household items. Architecture and integration of a mobile processor are driven by primary factors related to market and end-product. Some of these factors are Performance, Power, Cost and Size. We also have manufacturer preferences i.e. Thin modem -vs- fat modem; RF integration; system components and typically lower-tier products offer higher integration, but with less processing performance to reduce cost. The following are the past, present and what we expect in the future of mobile phones processor.

3. DIGITAL SIGNAL PROCESSORS

Digital signal processor (DSP) is a specialized microprocessor (or a SIP block), with its architecture optimized for the operational needs of digital signal processing. The goal of DSP is usually to measure, filter or compress continuous real-world analog signals. Most general-purpose microprocessors can also execute digital signal processing algorithms successfully, but may not be able to keep up with such processing continuously in real-time. Also, dedicated DSPs usually have better power efficiency, making them suitable in mobile phones because of power consumption constraints. DSPs often use special memory architectures that are able to fetch multiple data or instructions at the same time. DSPs became important with the transition from analog to digital cellular telephony. The first generation of cellular systems (called 1G systems) used analog transmission in the 1980s. Analog systems had the disadvantage of requiring more power for transmission, they allowed less users in the same band interval, and the handsets were usually bulky. In the early 1990s, analog cellular telephony was gradually substituted by second generation (2G) systems. The signal was not transmitted in analog form, it was previously converted into sequences of bits encoding the signal. Digital transmission allows the handset to compress the voice data, saving bandwidth. More complex control and connection protocols can be handled, and this allows to accommodate more users in the same frequency band. Moore's law, on the other side, allowed companies to build handsets which were smaller and smaller. The real explosion of cellular telephony started only with this second generation of digital devices.

The motor behind digital telephony are the DSPs. The first DSP was introduced by AT&T in 1979, but the most successful design came from a chip company, Texas Instruments. Ever since then, DSPs from Texas Instruments have dominated the market for digital telephony, and today 65% of the digital telephones use a chip made by TI. Traditionally, DSP used Harvard architecture which physically separates storage and signal pathway for instructions and data. This is in contrast with Von Neumann Architecture, where data and instructions are stored in the same memory. It has been said, that Digital Signal Processors (DSP) are to cellular telephones what the microprocessor is to desktop systems, that is, the heart of the whole design. We will examine how DSP architectures have evolved in the last years.

3.1 Traditional DSP (Digital Signal Processor) Architectures

3.1.1 Prototypical Architecture of a Mobile System

As the diagram shows below, there is a radio module which handles reception and transmission of digital signals. The RF interface handles the conversion of analog radio waves into bits, or vice versa for transmission. The bit stream is then passed to the DSP for speech or data decoding. The DSP can process the stream all by itself or can receive help from specialized chips (ASICs). A small microcontroller handles the user interface, the keyboard and LCD display, and the small operating system which orchestrates all services in the cellular handset. A flash memory is part of the system.

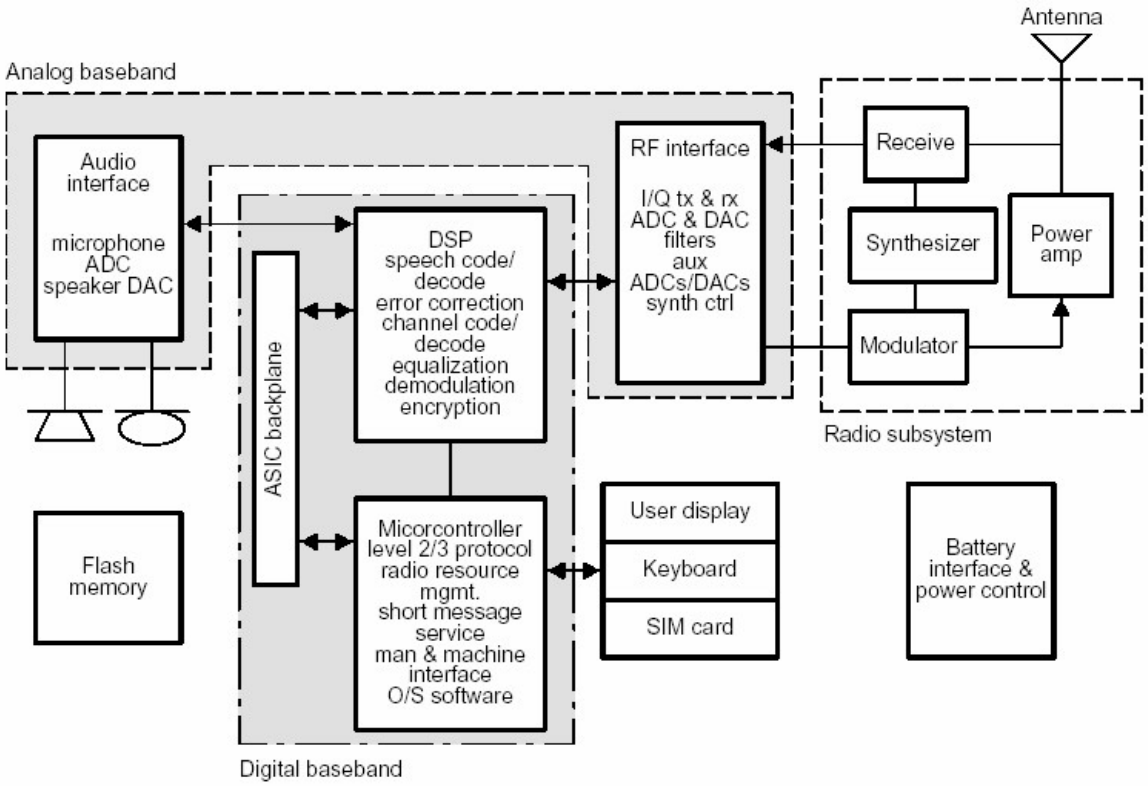

Figure 1: A cellular system of the second generation. A DSP handles all signal processing. A small, separate microcontroller, the user display, keyboard, and peripherals.

It can be used to store numbers, addresses, and other information. The audio interface handles the microphone and speakers. The kernel of the system is the DSP, as can be seen. A battery provides power to the system. A large memory space is not used, and virtual memory, for example is not needed. Memory for operation and storage is allocated in one single device (there are no hard-disks). The intelligence provided by the extra microcontroller is used to drive the few peripherals available, and the OS, but little else. In an MP3 player, the block architecture is very similar, but the whole radio subsystem is not needed, as well as the microphone. An MP3 player can be embedded in a cellular telephone at a minimal cost, and this is in fact what Nokia and other producers of cellular handsets have been doing in the last years.

3.1.2 Harvard Architecture

This architecture was named in remembrance of the Mark I computer built in 1944 at that university, Harvard. DSPs are designed for throughput. Digitized signals must go through the processor as fast as possible. Since at least an instruction is executed in every cycle, it is important to have a processor-memory bus for the program and one for the data. A Harvard architecture requires two output buses for the addresses generated for the processor: a data address and a code address. It requires additionally the read bus for code and a read/write bus for the data. The address bus for the code can be of limited width (24 bits, for example) since it is assumed that the code to be executed is not as large as in desktops. The read/write data bus can be designed to read a 32-bit word, but each 16-bit half-word can be treated internally as a separate argument. This allows the DSP to load two arguments into the processor in a single cycle. There is no cache for the instructions loaded into the processor, but there is a variety of buffers which can be used to speed up computations. In order to speed up access to memory, DSPs use registers which can be set and modified by address generation units. DSPs can have several different kinds of address units, for code or data. The motivation is always to speed up complications, that is, digital filtering.

3.1.3 Multiply-Accumulate ALU

Multiply-accumulate (MAC) is the kind of instruction most commonly associated with DSPs. When computing scalar product of vectors of length n, n pairs of numbers have to be multiplied pairwise and the partial results are added in a final result. In general purpose processors this is done using n multiplications and n additions, with load and store instructions in between. In a DSP the data path is laid out in such a way that the output of the multiplication unit connects directly to an adder, which adds and saves all partial results. In this way a scalar product of vectors of length n takes only n cycles. The MAC unit works in conjunction with the address generation units, so that in each cycle the two arguments needed are loaded directly from memory.

3.1.4 Zero-Overhead Looping

In digital signal processing there are operations over streams which can be implemented as loops of instructions. The loop is of fixed length and i.e. executed completely. Instead of testing a condition and branching if the end of the loop has not been reached, DSPs provide sets of special registers which count the iterations, are incremented automatically after each one, and which move the PC to the beginning of the loop when the loop body has been processed. The DSP execution units sees a linear flow of code without branches. This effect, which is achieved in RISC processor with the help of branch prediction and speculation, is achieved at a lower cost using the looping instructions of DSPs. DSPs provide many other special instructions, useful only in signal processing, such as those needed for Viterbi filtering, etc.

3.2. Modern DSP Architectures

Apart from traditional architectures, some modern DSP architectures have evolved for mobile devices such as TSM320C55 series and the TIGERSHARC.

3.2.1 The TMS320C55 series

TMS320C55 is a modern DSP architecture which implements Harvard architecture utilizing one and three read buses for code and data, respectively. Additionally, there are two write buses for data. Therefore, in the ideal case, this processor can read one instruction, read three operands, and write two results, all in the same cycle. The processor offers therefore extreme data-throughput, desirable and needed when processing streams of signals. Texas Instruments TMS320 is a blanket name for a series of digital signal processors (DSPs) from Texas Instruments. It was introduced on April 8, 1983 through the TMS32010 processor, which was then the fastest DSP on the market. The processor is available in many different variants, some with fixed-point arithmetic and some with floating point arithmetic.

The floating-point DSP TMS320C3x, which exploits delayed branch logic, has as many as three delay slots. The flexibility of this line of processors has led to it being used not merely as a co-processor for digital signal processing but also as a main CPU. Newer implementations support standard IEEE JTAG control for boundary scan and/or in-circuit debugging. The TMS32010 features separate address spaces for instruction and data memory but the ability to read data values from instruction memory. The TMS32010 featured a fast multiply-and-accumulate useful in both DSP applications as well as transformations used in computer graphics. The graphics controller card for the Apollo Computer DN570 Workstation, released in 1985, was based on the TMS32010 and could transform 20,000 2D vectors every second. TMS320C62XX is an example of VLIW (Very long instruction word) DSP processor. VLIW architecture in DSP provides a compiler-based programmer friendly environment. These VLIW processors follow explicitly parallel instruction computing (EPIC) architectures. TMS320C55 has programmable idle modes and automatic power saving features which bring down the processor frequency when the processor is not needed to perform at top speed.

3.2.2 The TIGERSHARC Architecture

The TigerSHARC is a DSP architecture developed by the company Analog Devices [Fridman 2000]. It has a series of advanced features, which correspond to the kind of DSP chips available in 2004 and few years after. The main innovation is the use of “short vectors” in order to process information in SIMD (single instruction multiple memory) manner. Although the TigerSHARC has only a clock frequency of 150 MHz (for saving power), it can deliver 3.6 GigaOPS (operations per second) working on 16-bit data. At these enormous processing rate, graphic processing for 3D applications becomes much easier. The TigerSHARC Processor's balanced architecture utilizes characteristics of RISC, VLIW, and DSP to provide a flexible, "all software" approach that adds capacity while reducing costs and bills of material. The TigerSHARC's unique ability to process up to 32-bit fixed-point as well as floating-point data types on a single chip allows original equipment manufacturers to adapt to evolving telecommunications standards without encountering the limitations of traditional hardware approaches that rely on ASICs, FPGAs, and ASSPs.

Having the highest performance DSP for communications infrastructure and multiprocessing applications available, TigerSHARC allows wireless infrastructure manufacturers to continue evolving their design to meet the needs of their target system, while deploying a highly optimized and effective Node B solution that will realize significant overall cost savings. The TigerSHARC Processor's balanced architecture optimizes system, cost, power, and density. A single TigerSHARC Processor, with its large on-chip memory, zero overhead DMA engine, large I/O throughput, and integrated multiprocessing support, has the necessary integration to be a complete node of a multiprocessing system.

This enables a multiprocessor network exclusively made up of TigerSHARCs without any expensive and power-consuming external memories or logic. TigerSHARC has up to four 32-bit instructions per cycle. It has large on-chip memory perfect for internal execution of up to 64,000-point FFTs.

3.3 System on Chip (SoC) based architectures

Mobile device processor architecture became simple with SOC designs. Real time responsiveness in mobile devices can be managed by using an enhanced DSP hybrid chip. Lowering the voltage of the chip enables low power operation in mobile devices. Matthias et al proposed a new scalable DSP architecture for SoC domains. In SoC based designs, system tasks can be managed by integrating microcontrollers, dedicated ASIC's, or DSP's in a single chip as shown in Figure 2 below:

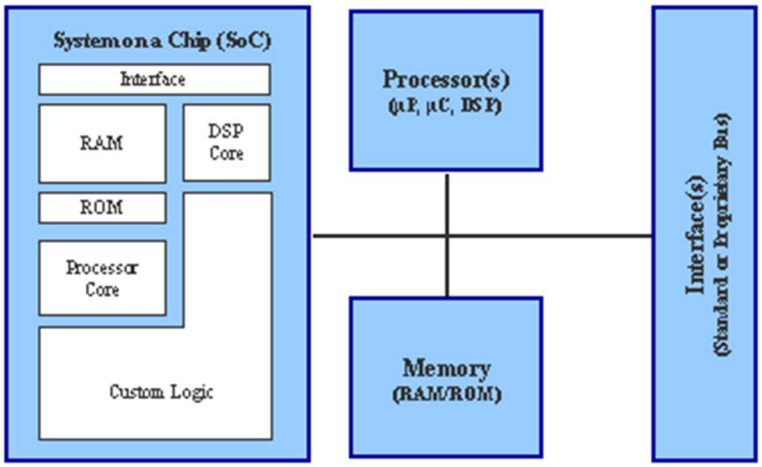

Figure 2: Traditional DSP Architecture (Harvard Architecture)

Highly integrated SoC's leveraging multicore technology has emerged for higher performance and low power designs. Low power operation often limits the architectural choices. High throughput of VLIW architectures in mobile devices requires a fast memory system like cache memories. To speed up the operation of mobile devices, instruction se customizations have been done by many companies. ARM Ltd. has done extensive instruction set customization by encoding most used instructions in 16-bit, so as to support more read-write operations. As we customize instruction set from 32-bit data types to 8-bit types, we are able to effectively improve memory utilization and the overall performance. Martin at el proposed reconfigurable processor architecture for mobile phones. Dynamically Configurable System on Chip (CSoC) architecture has been optimized for mobile communications. CSoC's are customized for a specific application and its architecture consists of processor core, memory, ASIC cores, and on-chip reconfigurable hardware units. Most of the smart phones today are single or dual-core SoC's. For most of the mobile applications, faster dual-core CPU provides better performance than quad-core SoC's. Future SoC's for mobile will become more sophisticated improving the overall performance.

3.4 ARM Processors

ARM based processors are the most widely used in modern Smart phones. ARM is a32-bit instruction set architecture based on RISC architecture. ARM processors are particularly used in Smart phones because of its low power consumption and great performance. ARM holdings provide chip design and instruction set customization licenses to third party vendors like Apple, Qualcomm etc. who design their own products based on the provided architecture. Various ARM architectures used in Smartphone are ARMv5 utilized in low-end devices, and ARMv6, ARMv7 utilized in recent high-performance devices. ARMv7 includes a hardware floating-point unit (FPU) providing improved speed. The 32-bit ARM architecture, such as ARMv7-A, is the most extensively used architecture in mobile devices. ARM architecture is the main hardware architecture for most of the operating systems of mobile devices such as iOS, Android, Windows Phone, Windows RT, Bada, Blackberry OS/Blackberry10, MeeGo, Firefox OS, Tizen, Ubuntu Touch, Sailfish and Igelle OS.

4. ARTIFICIAL INTELLIGENCE: THE FUTURE OF SMARTPHONES

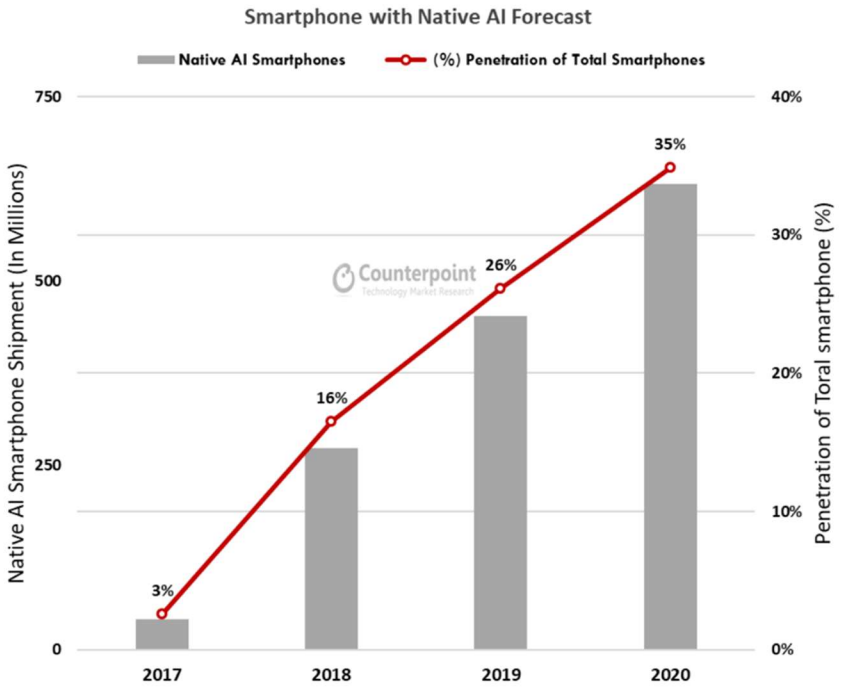

Fig 3: The number of smartphones shipping with dedicated AI processors forecast (Source: https://greenbookblog.org/wp-content/uploads/2019/02/rl1.png)

Artificial intelligence (AI) is an area of computer science that emphasizes the creation of intelligent machines that work and react like humans. Some of the activities computers with artificial intelligence are designed for include Speech recognition, Learning, Planning and Problem solving. Artificial intelligence (AI) is one of the most important recent developments in mobile phones. You'll hear the term all the time if you follow tech closely enough. Several new and recent phones have hardware optimized for AI.

These chips are usually called a **neural engine or neural processing unit**. They are designed for the fast processing of rapidly changing image data, which would use more processor bandwidth and power in a conventional chip. You'll find such a processor in the Huawei Mate 20 Pro's Kirin 980 CPU and the iPhone XS's A12 Bionic CPU. Qualcomm also added AI optimization to its Snapdragon 845 chipset, used in numerous high-end 2018 phones. These tweaks are particularly useful for camera-based AI, which tends to intersect with things like augmented reality and face recognition. A host of AI tasks are undertaken constantly in phones, already.

- **AI in the camera:** AI is already in the camera of most high-end smartphones, more than anywhere else. AI algorithms help identify whether you're snapping a panorama or a person – and adjusting the type of filtering used to give you the best results. It's likely AI also helps you by finding the right lens for the light conditions. AI is also behind the facial recognition you might use to get into your iPhone which, again, uses images from the onboard cameras. 'AI' is used to make a next-generation version of existing software seem more exciting.
- **AI in 'Siri' and other voice assistants:** Today's smartphones have basic Virtual Assistant capabilities which are improving rapidly. Some speech recognition now offers better levels of comprehension than a human listener, even in noisy environments. Virtual assistants are likely to become a much larger part of our interface with our phone, over time and the natural human language you provide is interpreted by AI.
- **Used to allow more human searches of images:** Many phones already automatically improve images (for example, removing red eye where it is found) and assist in sorting images you've taken and stored in your gallery in a human way – according to friend's names, for example. Some gallery software automatically pieces together a story of how your weekend went in the form of pictures taken on the day, animations and music.
- **AI key contributor to Augmented Reality experiences:** The targeted AI processors (often called Neural Processing Engines or something similar) that are found in these dedicated smartphone chips are also used by on-device Augmented Reality experiences, for example, Apple's Animoji.
- **Day to day operations:** More fundamentally, AI is behind Google's core search engine, every time you search from your phone and is being adapted to work behind the scenes in applications as battery life management and security.
- **Real conversations, by fake people:** Google also developed the most interesting, and unnerving, use for AI we've seen, in Google Duplex. This feature is part of Google Assistant, and lets it make calls on your behalf, to real people. It can try to book a table at a restaurant, or an appointment at a hair salon. Google showed off the feature at the I/O 2018 conference. And it was so creepily effective, the backlash caused Google to switch tactic and make Duplex tell the person on the other end it wasn't a real person.

5. DISCUSSION OF FINDINGS

- Mobile processor requirements are scaling exponentially
- Technology creates diversity
- Multicore solutions are required
- Artificial Intelligence is the future of Mobile Smartphones

6. CONCLUDING REMARKS

Different vendors are working towards the development of more power efficient mobile processor architectures by looking at the future of mobile computing. Software and the dedicated AI hardware required to run it efficiently is one way. Investments in the field of Artificial Intelligence in mobile phones has created a new 'battlefront' in the fight for customers. As such, many phone makers are queuing up to adopt Artificial Intelligence in an attempt to reinvent and deliver a more compelling user experience. It's not hard to see AI as the glue tying together the user interfaces on all of our internet interactions at some point in the near future. It already operates for us, behind the scenes, in ways that are not obvious to most technology consumers but which are becoming more mainstream by the day.

Mobile processing unit manufacturers are working hard to develop powerful cell phone devices. To support next-generation data-centric mobile devices, processor architecture has to be designed considering new approaches. Still, the development in mobile processors is driven by factors such as low-power consumption, user interface performance, time to market, etc.

7. CONTRIBUTIONS TO KNOWLEDGE

In light of the trends discussed so far, in order to improve more on processor architecture for mobile phones. The need for artificial intelligence chip integration is needed to meet the following needs;

- Need for higher CPU performance to provide enhanced mobile computing user experience
- Ability to create and play growing HD multimedia content
- Ability to handle multiple, high-speed data streams simultaneously

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