Advances in Mathematical & Computational Sciences Journal,
Vol. 7 No. 1, March 2019

Article Citation Format
Olujide A. Adenekan, Adeyemi I. Olateju & Mobolaji A. Sodunke (2019): Design And Implementation Of A Real Time Clock With Manual Set Using VHDL
Journal of Advances in Mathematical & Computational Sciences
Vol. 7, No. 1. Pp 71-76

Article Progress Time Stamps

Article Type: Research Article
Manuscript Received 19th Jan. 2019
Review Type: Blind
Final Acceptance: 27th March, 2019
Article DOI: dx.doi.org/10.22624/AIMS/MATHS/V7N1P9

Design and Implementation Of A Real Time Clock With Manual Set Using VHDL

Olujide A. Adenekan[1], Adeyemi I. Olateju[2] & Mobolaji A. Sodunke[3]
[1&2]Department of Computer Engineering, Moshood Abiola Polytechnic, Abeokuta, Nigeria
[3]Department of Science Laboratory Technology, Moshood Abiola Polytechnic, Abeokuta, Nigeria.
E-mails: adenekan.olujide@mapoly.edu.ng, olateju.adeyemi@mapoly.edu.ng
sodunke.mobolaji@mapoly.edu.ng

ABSTRACT

This paper presents a top – down design methodology for designing and implementation of a Real time clock (RTC) on a field programmable gate array (FPGA) using Very High-Speed Integrated Circuit Hardware Description Language (VHDL) in a Quartus II environment. The RTC module is sub divided into three modules namely the clock divider, the modulo counter and seven segment display modules. It has a functionality to display accurate time and the time can also be manually adjusted using appropriate switches on the FPGA board.

Keywords: Real time clock, FPGA, clock divider, VHDL

1. INTRODUCTION

Time is such an important concept, to the extent that it is exceptionally difficult to characterize. To measure time requires quantity that will repeat itself at regular interims. The quantity of interims checked gives a quantitative measure of the length of time. The early references for the estimation of the time are the moon and sun. At the point when the sun and the moon were not noticeable, it was difficult to know the precise time. Along these lines, timekeepers were created to allot the hours between the sun and the moon [1]. The procedure of measuring time has logically turned out to be more precise, and the gadgets more sophisticated from what is used in the early days. In the present day, the time is predominately measured by mechanical, and as of late by electronic timers. Truly, timers and clocks of various types lie at an imperative intersection of science, innovation, and society. Changes in timekeeping innovation have impacted the character of investigative perception, supported the improvement of other machine advances and noteworthy improvement is the way individuals consider and carry on in time [1] [2]. A clock is an instrument for measuring time. On a basic level, it requires some physical procedure occurring at a known rate, and an approach to measure to what extent that procedure has been occurring.

There are different types and sizes of clocks that are available in the market. Depending upon the format of

presentation, clocks can be classified into three categories namely (i) analogue clock (ii) Word clock (iii) digital clock. An analogue clock is a circular - faced clock with the numbers one to twelve around the outside and two hands, having a shorter one to measure hours and a longer one to measure minutes. A word clock is a clock signal used to synchronise other devices such as digital audio tape machines and compact disc players, which interconnect via digital audio signals. Digital clock shows a numeric representation of time. Two numeric characters arrangements are normally utilized on advanced clocks. They are: 24-hour documentation with hours running 00 to 23- and 12-hour documentation with AM/PM marker [2] [3].

A real time clock (RTC) is utilized to monitor the present time. In spite of the fact that the term frequently used to classify devices in PCs, servers and other devices, RTCs are available in any electronic gadget which needs to keep exact time for exact work to be kept up [4] [4].There are diverse advanced digital integrated circuits available in the market for designing digital circuits but as the systems gets complex there may be some capabilities that cannot be performed by these readily available ICs. Thus, the utilization of Very High-Speed Integrated Circuit Hardware Description Language (VHDL) for circuit design becomes very useful. For the programmable logic gadgets to be programmed the codes must go through some stages, for example, synthesis, simulation and route and generation [2] [5].

This work will be based on design and implementation on a real time clock on an Altera manufactured FPGA boards using manual set. The real time clock will display hour from (0-23) on seven segment display HEX 7-6, will display minutes from 0-59 and display it om HEX 5-4 and seconds will count 0-59 and displayed on HEX3-2 [6] [7]. There are several others manufacturers of FPGA board in the market such as Xilinx Inc, Perfect Parts Corporation, Achronix Semiconductor Corporation, Atmel Corporation to mention a few. It is a known fact that both Xilinx and Alter are very popular and have tools that are easy to use in addition to the University Program that both offer. But Altera is best known for simplicity and easy schematic entry [8].

2. REAL TIME CLOCK ALGORITHM DESIGN TIME COUNTING PROCESS

At start of the time counting procedure the hour, minute and second are set to zero. In the wake of passing every second, second is increased and checked in the event that it counts to fifty-nine. At the point when second surpasses fifty-nine then second is set to zero and minute is increased [9]. In the wake of passing one minute, it is checked if minute surpasses fifty-nine. At the point when minute surpasses fifty-nine then moment is set to zero and hour is incremented. In the wake of passing 60 minutes, it is checked if hour surpasses twenty-three. At the point when hour surpasses twenty-three then hour is set to zero and the process continue from start again[10] [11].

2.1 Manual time adjustment process

The main function of this process is time adjustment. The process begins involving pressing the reset key which return the hour, minutes and second on the display to zero segment display. Then the hour can be adjusted manually by using switches SW (15 DOWNTO 8) to input two- digit BCD numbers. By toggling the appropriate switches, the hour can be increased or decreased. Similar process for the hour adjustment is performed for the minute adjustment. The minutes can c be adjusted manually by using switches SW (7 DOWNTO 0) to input two-digit BC numbers. By toggling the appropriate switches, the hour can be increased or decreased.

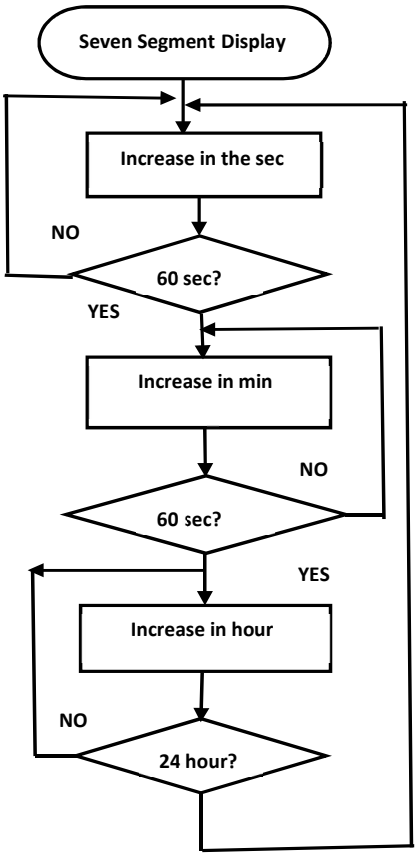

Figure 1: Time counting process for the RTC

2.3 VHDL implementation of real time clock

The code for all functionalities of the real time clock was designed using a hierarchical model. The top-level module (real time clock) module contains the full design entity which determines the function of the clock. The top-level module contains three sub modules namely:

1. The Clock Divider Module
2. The Modulo Counter Module
3. The Seven Segment Display Module

2.3.1 Clock Divider Section

The clock divider section of the real time clock contains the code which provides the clock pulse needed by the clock to work perfectly. The Altera DE2 -115 FPGA is designed to operate at a frequency of 50MHz. The 50MHz is not applicable for the timing in the digital clock; therefore, it needed to be reduced to the required value of 1Hz that is applicable for the digital clock. This was achieved by dividing the FPGA board oscillator frequency to obtain a frequency. This was done using the clock enable command as follows:

```
IF (CLOCK_50'EVENT AND CLOCK_50 = '1') THEN
slow_count <= slow_count + '1';
```

2.3.2 The Modulo counter Section

This section of the design contains the codes for the counter. The signals E_hr_ 0 and E_hr_ 1 representing the two numeric character hour of the clock and E_min_0 and E_min _1 representing two numeric characters of the minutes of the clock are all produced inside modulo counter. These signals are driven by a clock frequency of approximately 1Hz.The time counting process for the clock is as follows. When the clock pulse is high E_min_0 value is increased by 1. E_min_0 can count from 0 to 5 then it start counting from zero up. E_min_1 can count from 0 to 9, then it go back to 0 and start counting up to 9. E_hr_0 can only count from 0 to 2 then start from 0 again. E_hr_1 can count from 0 to 9 then it will start counting from 0. If the value of E_hr _1 is more than 3 and the value of E_hr_0 is 2. This will cause the value of both E_hr_0. For every rising edge of the clock pulse the second signal is increased by 1. In summary it can be explained as follows when the seconds signal counts up to 59. The minute is incremented by and the seconds signal return to 0. When the minute signal counts to 59; the hour is increased by 1. This process continues until the hour count up to 23 and all the values of the hour, minute and second returns back to zero.

2.3.3 The seven-segment display section contains

This section contains the codes that drives the display of the seven-segment display of the FPGA. The BCD output signal from the counter is port map on the component bcd7seg and the output is displayed as the time on seven segment display HEX 7-2. The seven-segment display HEX1-0 WAS blanked out.

2.4 Flow Summary of the Design

The flow summary of the process is shown the figure below. It flows process was successful and we can also see that the less that 1% of the total logic element was utilized in the design.

Flow Summary	
Flow Status	Successful - Thu Dec 17 20:49:05 2015
Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Full Version
Revision Name	realtimeclock
Top-level Entity Name	realtimeclock
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	142 / 114,480 (< 1 %)
Total combinational functions	139 / 114,480 (< 1 %)
Dedicated logic registers	49 / 114,480 (< 1 %)
Total registers	49
Total pins	77 / 529 (15 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

Figure 2: Shows the Flow Summary

3. RESULTS

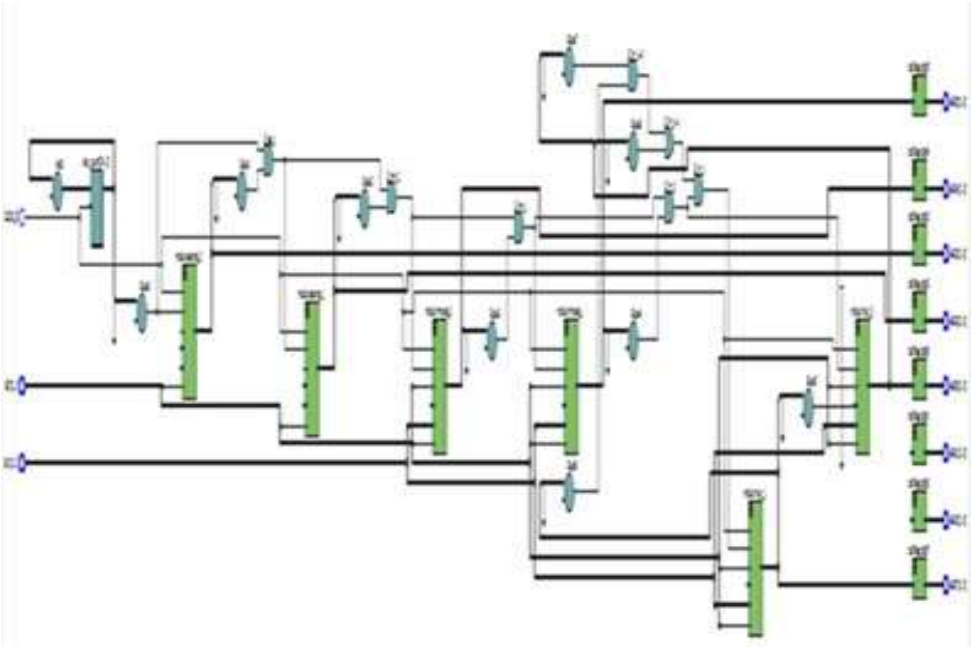

Figure 3: Illustrates the bird view of the register transfer level

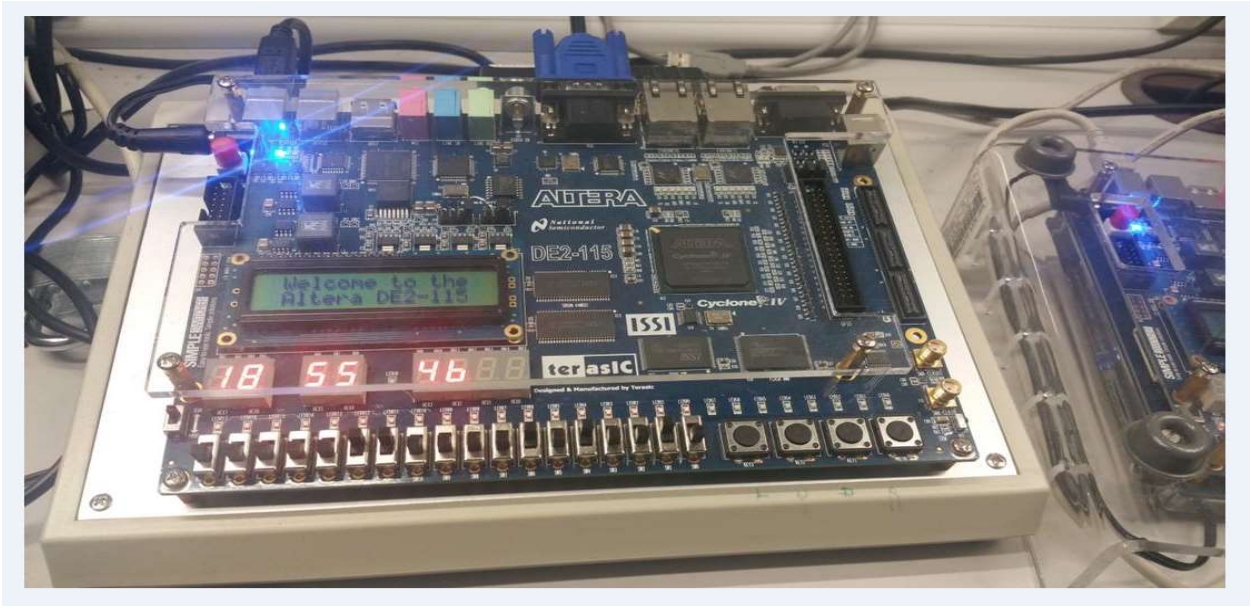

Figure 4: Depict the implementation of the real time clock on the FPGA (Altera DE2115) board

4. CONCLUSION

The real time clock was designed and implemented using VHDL and the code was compiled using Quartus 15 software. Necessary pin assignment was done to implement the circuit on the board. The VHDL file passes the synthesis without any error. The bit was generated and downloaded onto the Altera DE2115 board to test the functionality of the clock. The circuit performed the required function as specified in figure 4 and deducing the flow summary it can be seen that the resources are efficiently utilized.

REFERENCES

1. Pantec Solutions , "pantec Solution," www.pantechsolutions.net , [Online]. Available: http://www.pantechsolutions.net . [Accessed 25 November 2015].
2. S. S. Usman Sammani and S. . H. Ibrahim, "Design of a Digital Clock Using Very High Speed ICHardware Description Language," *AKGEC INTERNATIONAL JOURNAL OF TECHNOLOGY,* vol. 6, no. 1, pp. 1-3, 2015.
3. I. S. Mominul, K. M. Humayun, K. M. Zahidul , A., M. Tanvir and N. Muslim, "Design and implementation of a digital clock showing digits in Bangla font using microcontroller AT89C4051," eprint arXiv:1208.0995, 08/2012.
4. K. R. Sadeque , K. Alvir and H. . A. Dilshad , "Designing Smart Multipurpose Digital Clock using Real Time Clock (RTC) and PIC Microcontroller," *International Journal of Computer Applications (0975 – 8887),* vol. 41, no. 9, pp. 39-41, March 2012.
5. S. Areibi, "A first course in digital design using VHDL and programmable logic," *Frontiers in Education Conference, 2001. 31st Annual,* vol. 1, pp. TIC - 19-23 vol.1, 2001.
6. Real-Time Clocks (RTC) ICs - Maxim", Maximintegrated.com, 2016. [Online]. Available:https://www.maximintegrated.com/en/products/digital/real-time-clocks.html. [Accessed: 27- Feb-2018].
7. Javier Jalle, Mikel Fernandez, Jaume Abella, Jan Andersson, Mathieu Patte, Luca Fossati Marco Zulianello, Francisco J. Cazorla,"Contention-Aware Performance Monitoring Counter Support for Real-Time MPSoCs", 2016.
8. Mohd Alias, M.N.A., Mohyar, S.N. "Architectural design proposal for a real-time clock for Wireless microcontroller unit" (2017) EPJ Web of Conferences, 162, art. no. 01072.
9. David Ruffieux, Franz Pengg, Nicola Scolari, Frédéric Giroud, Daniel Severac, Thanh Le, Silvio Dalla Piazza, Olivier Aubry, "11.5 A 3.2×1.5×0.8mm3 240nA 1.25-to-5.5V 32kHz- DTCXO RTC module with an overall accuracy of µ1ppm and an all-digital 0.1ppm compensation-resolution scheme at 1Hz", 2016 IEEE International Solid-State Circuits Conference (ISSCC), 31 Jan.-4 Feb. 2016, San Francisco, CA, USA.
10. Ju-Hyun Park, Sung Han Do, Sung Jin Kim, Ho-Cheol Ryu, and Kang-Yoon Lee, "A Design of 4.19MHz Real Time Clock Generator with Triple mode for Fast settling, Current Reduction and Low Noise in 0.18um CMOS ", 2016.
11. Pyoungwon Park, David Ruffieux, and Kofi A. A. Makinwa, "A Thermistor-Based Temperature Sensor for a Real- Time Clock With 2 ppm Frequency Stability ", IEEE Journal of Solid-State Circuits (JSCC), Vol. 50, No. 7, 2015.